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09/870,280	05/30/2001	Mojdeh Shakeri	04899-050001	7303

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,280	SHAKERI ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 were examined.

Section I: Non-Final Rejection (5th Office Action)

Claim Interpretation

2. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. The Office defines a tree structure as follows (source-- *www. Dictionary.com*): Computer Science. A structure for organizing or classifying data in which every item can be traced to a single origin through a unique path.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-36 are rejected under 35 U.S.C. 101 because the limitations reflect non-statutory subject matter involving signal theory with no specific application. For example, the specification on page 7, lines 6-21, claim no specific application to which the signal block identities and applications are unknown. If a claimed process manipulates only numbers, abstract concepts or ideas, or signals representing any of the foregoing, the claim is not being applied to appropriate subject matter. Schrader, 22 F.3d at 294-95, 30 USPQ2d at 1458-59. The Federal Circuit also recognizes that the fact that a nonstatutory method is carried out on a programmed computer does not make the process claim statutory. Grams, 888 F.2d at 841, 12 USPQ2d at 1829 (claim 16 ruled nonstatutory even though it was a computer- implemented process).

A product is a tangible physical article or object, some form of matter, which a signal is not. That the other two product classes, machine and composition of matter, require physical matter is evidence that a manufacture was also intended to require physical matter. *A signal, a form of energy, does not fall within either of the two definitions of manufacture. Thus, a signal does not fall within one of the four statutory classes of § 101.*

On the other hand, from a technological standpoint, a signal encoded with functional descriptive material is similar to a computer-readable memory encoded with functional descriptive material, in that they both create a functional interrelationship

with a computer. In other words, a computer is able to execute the encoded functions, regardless of whether the format is a disk or a signal.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2 and 8-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Matlab News & Notes (February 2000; hereafter MNN). MNN teaches compiling graphical user interfaces and graphics by using C++ compiler suite (pg.1).

Claim 1. A modeling process comprising: providing a plurality of blocks (pg. 13, figure 5), each of the blocks representing functional entities (pg. 13, figure 5) that operate on a plurality of input signal values ("complex exponential" and "signal input" into modulate signal, pg. 13, figure 5); generating a plurality of output signal values from the plurality of blocks (the real and imaginary signals from the demodulate block, pg. 13, figure 5); grouping the plurality of output signal values (the real and imaginary signals from the demodulate block, pg. 13, figure 5) as an ordered set in a multiplexer as a first composite signal; and outputting the first composite signal (output from "modulate" block, pg. 13, figure 5).

Claim 2. The process of claim 1 wherein each of the blocks includes at least one input signal port (pg. 13, figure 3, inputs to "modulate" block and its one output) and at least one output signal port.

Claim 8. The process of claim 1 wherein the ordered set is a linked list data structure (e.g., algorithm, pg. 18, right column, "Signal Master" section, line 10).

Claim 9. The process of claim 8 wherein the linked list data structure is a tree data structure (see claim interpretation with figure 5, pg. 13) to the tree data structure including m+n nodes.

Claim 10. The process of claim 9 wherein m represents a number of independent signals and n represents a number of composite signals (output from "modulate" block, pg. 13, figure 5).

Claim 11. The process of claim 1 further comprising decomposing the first composite signal (output from "modulate" block, pg. 13, figure 5 as a first composite signal) into the plurality of output signals in a demultiplexer.

Claim 12. The process of claim 1 further comprising viewing the ordered set contained in the first composite signal (output from "modulate" block, pg. 13, figure 5 as a first composite signal) with a composite signal viewer.

Claim 13. The process of claim 1 wherein at least one of the input signal values is a second composite signal (output from "demodulate" block, pg. 13, figure 5 as a second composite signal).

Claim 14. A block diagram (pg. 13, figure 5) modeling process comprising: providing a first block and a second block ("input signal block" as the first; "complex signal block" as the second: pg. 13, figure 5), the blocks representing functional entities that operate on a plurality of input signal values (pg. 13, figure 5); generating a plurality of output signal values from the first and second block ("input signal block" as the first; "complex signal block" as the second: pg. 13, figure 5); grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (output from "modulate" block, pg. 13, figure 5); and processing the composite signal in a third block ("modulate block" as the third block.

Claim 15. The process of claim 14 wherein the ordered set is a linked list data structure (e.g., an algorithm, pg. 18, right column, "Signal Master" section, line 10).

Claim 16. The process of claim 14 wherein at least one of the input signals is a second composite signal (output from "demodulate" block, pg. 13, figure 5).

Claim 17. The process of claim 14 further comprising decomposing the composite signal (output from "modulate" block, pg. 13, figure 5) into the plurality of input signal

values.

Claim 18. The process of claim 14 further comprising viewing the composite signal (output from "modulate" block, pg. 13, figure 5) in a composite signal viewer.

Claim 19. The process of claim 18 wherein the composite signal viewer displays the ordered set contained in the composite signal (output from "modulate" block, pg. 13, figure 5)on a graphical user interface (GUI) (pg. 6, left column, 3rd paragraph, line 5).

Claim 20. The process of claim 19 wherein the GUI (pg. 6, left column, 3rd paragraph, line 5) is provided on an input/output device.

Claim 21. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor (pg. 18, "Turbo Code and Viterbi Decoders" section), cause the processor to: provide a plurality of blocks (pg. 13, figure 5), each of the blocks representing functional entities that operate on a plurality of input signal values (signals into the modulate, pg. 13, figure 5); generate a plurality of output signal values from the plurality of blocks ("the real and imaginary double signals" pg.13, figure 5); group the plurality of output signal values (the real and imaginary signals from the demodulate block, pg. 13, figure 5) as an ordered set in a multiplexer as a first composite signal; and output the first composite signal (output from "modulate" block, pg. 13, figure 5).

Claim 22. The computer program product of claim 21 wherein the computer readable medium is a random access memory (RAM) (well known).

Claim 23. The computer program product of claim 21 wherein the computer readable medium is read only memory (ROM) (well known).

Claim 24. The computer program product of claim 21 wherein the computer readable medium is hard disk drive (well known).

Claim 25. A processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and a memory ("parts of a computer"—well known) configured to: provide a plurality of blocks, ("the real and imaginary double signals" pg.13, figure 5) each of the blocks representing functional entities that operate on a plurality of input signal values (signals into the modulate, pg. 13, figure 5); generate a plurality of output signal values from the plurality of blocks (the real and imaginary signals from the demodulate block, pg. 13, figure 5); group the plurality of output signal values(the real and imaginary signals from the demodulate block, pg. 13, figure 5) as an ordered set in a multiplexer as a first composite signal; and output the first composite signal (signal from complex exponential to demodulate box, figure 5, pg 13).

Claim 26. The processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and memory of claim 25 wherein the processor (pg. 18, "Turbo Code and Viterbi Decoders"

section) and the memory are incorporated into a personal computer (well known).

Claim 27. The processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and memory of claim 25 wherein the processor and the memory are incorporated into a network server residing in the Internet (well known).

Claim 28. The processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and memory of claim 25 wherein the processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and the memory are incorporated into a single board computer (well known).

Claim 29. A modeling process comprising: providing a plurality of blocks, ("the real and imaginary double signals" pg.13, figure 5) each of the blocks representing a functional entity that operates on one or more input signal values ("the real and imaginary double signals" pg.13, figure 5) and generates one or more output signals; grouping the output signals use an ordered set in a multiplexer as a composite signal ("the real and imaginary double signals" pg.13, figure 5); and outputting the composite signal (output from modulate box, pg. 13, figure 5).

Claim 30. The process of claim 29 wherein the ordered set is a tree data structure (see claim interpretation with figure 5, pg. 13).

Claim 31. The process of claim 30 wherein the tree data structure (see claim interpretation with figure 5, pg. 13) is a linked list.

Claim 32. The process of claim 29 further comprising: providing a composite signal viewer; and viewing the ordered set in a graphical user interface (pg. 6, left column, 3rd paragraph, line 5) executing in the composite signal viewer.

Claim 33. A computer program product residing on a computer readable medium ("PC" personal computer, pg. 6, "Rapid Development, Reliable Deployment" section, 3rd paragraph, last sentence) having instructions stored thereon which, when executed by the processor, (pg. 18, "Turbo Code and Viterbi Decoders" section) cause the processor to: provide a plurality of blocks (pg. 13, figure 5), each of the blocks representing a functional entity that operates on one or more input signal values (pg. 13, figure 5) and generates one or more output signal values (demodulate block, pg. 13, figure 5); group the output signals as an ordered set in a multiplexer as a composite signal; and output the composite signal (output from modulate box, pg. 13, figure 5).

Claim 34. A processor (pg. 18, "Turbo Code and Viterbi Decoders" section) and memory configured to provide a plurality of blocks, each of the blocks representing a functional entity (i.e., "modulate", "demodulate", etc., pg. 13, figure 5) that operates on one or more input signal values (pg. 13, figure 5) and generates one or more output signal values; group the output signals as an ordered set in a multiplexer as a composite signal (output from modulate box, pg. 13, figure 5); and output the composite signal (output from modulate box, pg. 13, figure 5).

Claim 35. A method for providing a composite signal (output from "modulate" block, pg. 13, figure 5) in a modeling environment, the method comprising the steps of: providing a plurality of output signals from one or more blocks ("complex exponential" and "signal input" into modulate signal, pg. 13, figure 5); generating a composite signal (output from "modulate" block, pg. 13, figure 5) comprising a set of the plurality of output signals (output from "modulate" block, pg. 13, figure 5); and providing the composite signal as an output signals (output from "modulate" block, pg. 13, figure 5).

Claim 36. A method for graphically representing a composite signal in a modeling environment, the method comprising the steps of: providing a plurality of output signals from one or more blocks, each output signal graphically indicated by a signal identifier (e.g., sine, cosine, pg. 13, equations left column); and providing a composite signal (output from modulate box, pg. 13, figure 5) identifier to graphically indicate a grouping of signal identifiers, the composite signal (output from modulate box, pg. 13, figure 5) identifier representing a composite signal (output from modulate box, pg. 13, figure 5) comprising a set of the plurality of output signals.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over MNN discloses attributes, amplitude/phase/frequency (characteristics of a sine wave, pg. 11, figure 2), and dimensions (pg. 6, left column, 3rd paragraph, lines 5-8).

The MNN reference does not expressly teach discloses attributes, amplitude/phase/frequency and dimensions.

10. Official notice is taken that attributes, amplitude/phase/frequency, and dimensions are well known at the time of invention was made in the analogous art of graphical illustrations of sinusoidal signals processing analysis.

At the time of invention was made, it would have been obvious to a person of ordinary skill in the art to label the output signals as part of graphically illustrating the results within a GUI interface.

The suggestion to do so would have been obvious in order to create sophisticated GUIs to display 2D and 3D results (pg. 6, left column, 3rd paragraph, lines 5-8).

Therefore, it would have been obvious to modify MNN to obtain the invention as specified in claims 2-7.

Section II: Response to Applicants' Arguments

101

11. Applicants are thanked for addressing this issue; however, the applicants' response is non-persuasive to negate the rejection. The claims are a mere listing of function steps without a concrete or tangible result. The graphical depiction of composite signals on a GUI interface (e.g., claims 1-9) fail to denote a specific, credible end result; an "outputting the first composite signal" (e.g., claim 1) is not considered credible. In fact, the limitations read on mathematical concepts (i.e., discrete data values; and composite signal values) that are obvious to any 3rd year electrical

engineering student modeling sinusoidal signal processing (e.g., Matlab's Simulink software).

Applicants argued the invention's usefulness, stating the "model execution speed... improves modeling cycle times" which is credible and specific; however, the claims are silent on these features.

Applicants provide several examples of real-world applications for this invention (applicants' arguments, page 8, lines 15-20), to which none are disclosed within the original disclosure.

Legally, the claims are manipulating abstract numbers that lack a clear and concise application. Rejection stands.

Citation to Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Bishop,R.H., "Modern Control Systems Analysis & Design" 1997, Univ of Texas (Austin), pg. 4-5, 7-15, and 96-100; teaches modern control signal simulation programs.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

July 3, 2006

TS

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7/10/06